AMENDMENTS TO THE CLAIMS

For the convenience of the Examiner, all claims have been presented whether or not an amendment has been made. The claims have been amended as follows:

1. **(Currently Amended)** A receiver, comprising:

a discriminator unit configured to receive an over-sampled data signal as an input; and

a timing recovery unit configured to align a clock signal outputted by a free-running clock with a received data signal present in the over-sampled data signal to extract data therefrom, wherein an output signal of the discriminator unit is provided as an input to the timing recovery unit~~;~~.

wherein the timing recovery unit further comprises:

an edge detector coupled to receive the output signal of the discriminator unit and adapted to detect a rising edge of the output signal;

a comparator coupled to receive an output of the edge detector and a recovered clock signal extracted from the over-sampled data signal and adapted to compare the received clock signal and received data signal to determine whether the rising edge of the recovered clock signal aligns with a midpoint of the received data signal; and

an edge shifter coupled to receive the output of the edge detector and adapted to advance the recovered clock signal in time when the rising edge of the recovered clock signal is proximate a falling edge of the received data signal and to delay the recovered clock signal when the rising edge of the recovered clock signal is proximate a rising edge of the received data signal.

2. **(Canceled)**

3. **(Currently Amended)** The receiver of **claim 1** ~~claim 2~~, wherein the edge detector further comprises:

an XOR gate having a first input and a second input, the first input coupled to receive the output signal of the discriminator unit; and

a signal delay unit coupled to receive the output signal of the discriminator unit and the free-running clock signal, and to output a delayed signal to the second input of the XOR gate.

4. **(Currently Amended)** The receiver of **claim 1** ~~claim 2~~, wherein the comparator further comprises:

a first AND gate having a first input and a second input, the first input coupled to receive the output of the edge detector; and

a counter coupled to provide a signal to the second input of the first AND gate when a pre-determined threshold value is met or exceeded.

5. **(Currently Amended)** The receiver of **claim 1** ~~claim 2~~, wherein the edge shifter further comprises:

a counter;

a first and second AND gates each coupled with the second counter, an output of the first AND gate to advance a first input of the counter so as to advance the counter by one cycle when the rising edge of the recovered clock signal is proximate a falling edge of the received data signal, an output of the second AND gate coupled to a second input of the counter so as to delay the counter by one cycle when the rising edge of the recovered clock signal is proximate a rising edge of the received data signal.

6. **(Original)** A digital circuit, comprising:

a receiving unit coupled to receive a data signal and a clock signal;

an edge detector coupled to receive an output from the receiving unit and configured to detect a rising edge of the clock signal;

a comparator coupled to the edge detector and configured to compare the clock signal and the data signal to determine whether the rising edge of the clock signal aligns with a midpoint of the data signal; and

an edge shifter coupled to the edge detector and configured to advance the data signal in time when the rising edge of the clock signal is proximate a falling edge of the data signal and to delay the data signal in time when the rising edge of the clock signal is proximate a rising edge of the data signal.

7. **(Original)** The digital circuit of claim 6, wherein the edge detector further comprises:

an XOR gate having a first input and a second input, the first input coupled to receive the data signal; and

a signal delay unit coupled to receive the data signal and the clock signal, and configured to output a delayed data signal to the second input of the XOR gate.

8. **(Original)** The digital circuit of claim 6, wherein the comparator further comprises:

an AND gate having a first input and a second input, the first input coupled to receive the output of the edge detector; and

a counter coupled to provide a signal to the second input of the AND gate when a pre-determined threshold value is met or exceeded.

9. **(Currently Amended)** The digital circuit of claim 6, wherein the edge shifter further comprises:

a counter; **and**

~~a first~~ **first** and second AND gates ~~each coupled to the counter~~, **wherein** an output of the first AND gate **is** coupled to ~~a first input of~~ the counter so as to advance the ~~second~~ counter by one cycle when the rising edge of the clock signal is proximate a falling edge of the data signal, **and** an output of the second AND gate **is coupled to the counter** to delay the counter by one cycle when the rising edge at the clock signal is proximate a rising edge of the data signal.

10. **(Currently Amended)** A method, comprising:

directly downconverting a radio frequency signal to produce in-phase and quadrature components thereof and filtering the in-phase and quadrature components to produce a pair of received signals;

demodulating the pair of received signals among a discriminator configured to extract an over-sampled data signal from the pair of received signals and a timing recovery unit configured to align a clock signal generated by a free-running clock with a moving edge of the over-sampled data signal to produce a bit-timing clock used to extract a data signal from the over-sampled data signal;

wherein the discriminator extracts the over-sampled data signal by logically XORing bit-stored versions of the received signal and the delayed replicas of themselves and filtering a resulting signal.

11. **(Canceled)**

12. **(Currently Amended)** The method of **claim 10** ~~claim 11~~, wherein the filtering of the resulting signal is performed using a low pass filter.

13. **(Currently Amended)** The method of **claim 10** ~~claim 11~~, wherein the filtering of the resulting signal is performed using a digital implementation of a low pass filter.

14. **(Original)** The method of claim 13, wherein the digital implementation of the low pass filter accumulates counts of shift registers until a threshold value is reached.

15. **(Original)** The method of claim 10 wherein the timing recovery unit produces the bit-timing clock by adjusting the free-running clock in time using a counter.

16. **(Original)** The method of claim 15, wherein the timing recovery unit extracts the data signal by compressing a leading edge of the over-sampled data signal to the bit-timing clock.

17. **(Original)** The method of claim 16, wherein a comparison of the bit-timing clock and the leading edge of the over-sampled data signal causes a shifting in time of the over-sampled data signal so as to ensure the over-sampled data signal is itself sampled to provide valid data.

18. **(Currently Amended)** The method of claim 10, wherein direct ~~downcoversion~~ **downconversion** of the radio-frequency signal results in production of an intermediate signal of a frequency higher than a base-band frequency.

19. **(Original)** The method of claim 10 wherein direct downconversion of the radio-frequency signal results in a base-band signal.

20. **(Original)** The method of claim 10, wherein direct downconversion of the radio frequency signal and demodulation of the pair of received signals is accomplished using a system on-a-chip receiver.

21. **(New)** A method, comprising:

directly downconverting a radio frequency signal to produce in-phase and quadrature components thereof and filtering the in-phase and quadrature components to produce a pair of received signals;

demodulating the pair of received signals among a discriminator configured to extract an over-sampled data signal from the pair of received signals and a timing recovery unit configured to align a clock signal generated by a free-running clock with a moving edge of the over-sampled data signal to produce a bit-timing clock used to extract a data signal from the over-sampled data signal;

wherein the timing recovery unit produces the bit-timing clock by adjusting the free-running clock in time using a counter, and the timing recovery unit extracts the data signal by compressing a leading edge of the over-sampled data signal to the bit-timing clock.